WHAT IS CLAIMED IS:

1. A write strategy circuit for capturing input data to be written on an optical disk, comprising:

a strategy clock generator configured to generate a strategy clock signal by multiplying a frequency of a channel clock signal;

a phase controller configured to produce a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal;

a data capturing circuit configured to capture the input data in synchronization with the capturing channel clock signal;

a phase determination circuit configured to determine whether a length of the input data corresponds to a predetermined value; and

a strategy correction circuit configured to apply a predetermined strategy correction to the input data based on the strategy clock signal,

wherein the phase controller controls the phase of the channel clock signal according to a determination result of the phase determination circuit.

2. A write strategy circuit as claimed in Claim 1,

wherein the phase controller generates a plurality of clock signals having different phases by sequentially shifting the phase of the channel clock signal based on a cycle of the strategy clock signal, and selects one of the plurality of clock signals as the capturing channel clock signal according to the determination result.

3. A write strategy circuit as claimed in Claim 1, further comprising:

a PLL circuit configured to generate the strategy clock signal based on the channel clock signal; and

a frequency divider configured to convert the strategy clock signal to an output signal having a frequency substantially equal to the frequency of the channel clock signal.

4. A write strategy circuit as claimed in Claim 3, wherein the phase controller produces the capturing channel clock signal by controlling a phase of the output signal according to the determination result.

5. A write strategy circuit as claimed in Claim 1, further comprising a memory for storing the determination result,

wherein the phase determination circuit stores the determination result in the memory, and the phase controller controls the phase of the channel clock signal according to the determination result stored in the memory.

6. A write strategy method for capturing input data to be written on an optical disk, comprising the steps of:

first generating a strategy clock signal by multiplying a frequency of a channel clock signal;

first producing a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal;

capturing the input data in synchronization with the capturing channel clock signal;

determining whether a length of the input data corresponds to a predetermined value; and

applying a predetermined strategy correction to the input data based on the strategy clock signal,

wherein the first producing step controls the phase of the channel clock signal according to a determination result of the determining step.

7. A write strategy method as claimed in Claim 6, further comprising the steps of:

second generating a plurality of clock signals having different phases by sequentially shifting the phase of the channel clock signal based on a cycle period of the strategy clock signal; and

selecting one of the plurality of clock signals as the capturing channel clock signal according to the determination result.

8. A write strategy method as claimed in Claim 6, further comprising the steps of:

third generating the strategy clock signal based on the channel clock signal; and

converting the strategy clock signal to an output signal having a frequency substantially equal to the frequency of the channel clock signal.

9. A write strategy method as claimed in Claim 8, further comprising the step of:

second producing the capturing channel clock signal by controlling a phase of the output signal according to the determination result.

10. A write strategy method as claimed in Claim 6, further comprising the step of storing the determination result,

wherein the first producing step controls the phase of the channel clock signal according to the determination result.

11. A write strategy circuit for capturing input data to be written on an optical disk, comprising:

first generating means for generating a strategy clock signal by multiplying a frequency of a channel clock signal;

first producing means for producing a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal;

means for capturing the input data in synchronization with the capturing channel clock signal;

determining means for determining whether a length of the input data corresponds to a predetermined value; and

means for applying a predetermine strategy correction to the input data based on the strategy clock signal,

wherein the first producing means controls the phase of the channel clock signal according to a determination result of the determining means.

12. A write strategy circuit as claimed in Claim 11, further comprising:

second generating means for generating a plurality of clock signals having different phases by sequentially shifting the phase of the channel clock signal based on a cycle of the strategy clock signal; and

selecting means for selecting one of the plurality of clock signals as the capturing channel clock signal according to the determination result.

13. A write strategy circuit as claimed in Claim 11, further comprising:

third generating means for generating the strategy clock signal based on the channel clock signal; and

means for converting the strategy clock signal to an output signal having a frequency substantially equal to the frequency of the channel clock signal.

14. A write strategy circuit as claimed in Claim 13, further comprising:

second producing means for producing the capturing channel clock signal by controlling a phase of the output signal according to the determination result.

15. A write strategy circuit as claimed in Claim 11, further comprising means for storing the determination result,

wherein the first producing means controls the phase of the channel clock signal according to the determination result.

16. An optical disk apparatus for capturing input data to be written on an optical disk, comprising a write strategy circuit including:

a strategy clock generator configured to generate a strategy clock signal by multiplying a frequency of a channel clock signal;

a phase controller configured to produce a capturing channel clock signal by controlling a phase of the channel clock signal in synchronization with the strategy clock signal;

a data capturing circuit configured to capture the input data in synchronization with the capturing channel clock signal;

a phase determination circuit configured to determine whether a length of the input data corresponds to a predetermined value; and

a strategy correction circuit configured to apply a predetermined strategy correction to the input data based on the strategy clock signal,

wherein the phase controller controls the phase of the channel clock signal according to a determination result of the phase determination circuit.

17. An optical disk apparatus as claimed in Claim 16, wherein the phase controller generates a plurality of clock signals having different phases by sequentially shifting the phase of the channel clock signal based on a cycle of the strategy clock signal, and selects one of the plurality of clock signals as the capturing channel clock signal according to the determination result.

18. An optical disk apparatus as claimed in Claim 16, wherein the write strategy circuit further comprises:

a PLL circuit configured to generate the strategy clock signal based on the channel clock signal; and

a frequency divider configured to convert the strategy clock signal to an output signal having a

frequency substantially equal to the frequency of the channel clock signal.

19. An optical disk apparatus as claimed in Claim 18,

wherein the phase controller produces the capturing channel clock signal by controlling a phase of the output signal according to the determination result.

20. An optical disk apparatus as claimed in Claim 16, wherein the write strategy circuit further comprises a memory for storing the determination result, and

wherein the phase determination circuit stores the determination result in the memory, and the phase controller controls the phase of the channel clock signal according to the determination result stored in the memory.